Hybrid Correlator for VLBI2010

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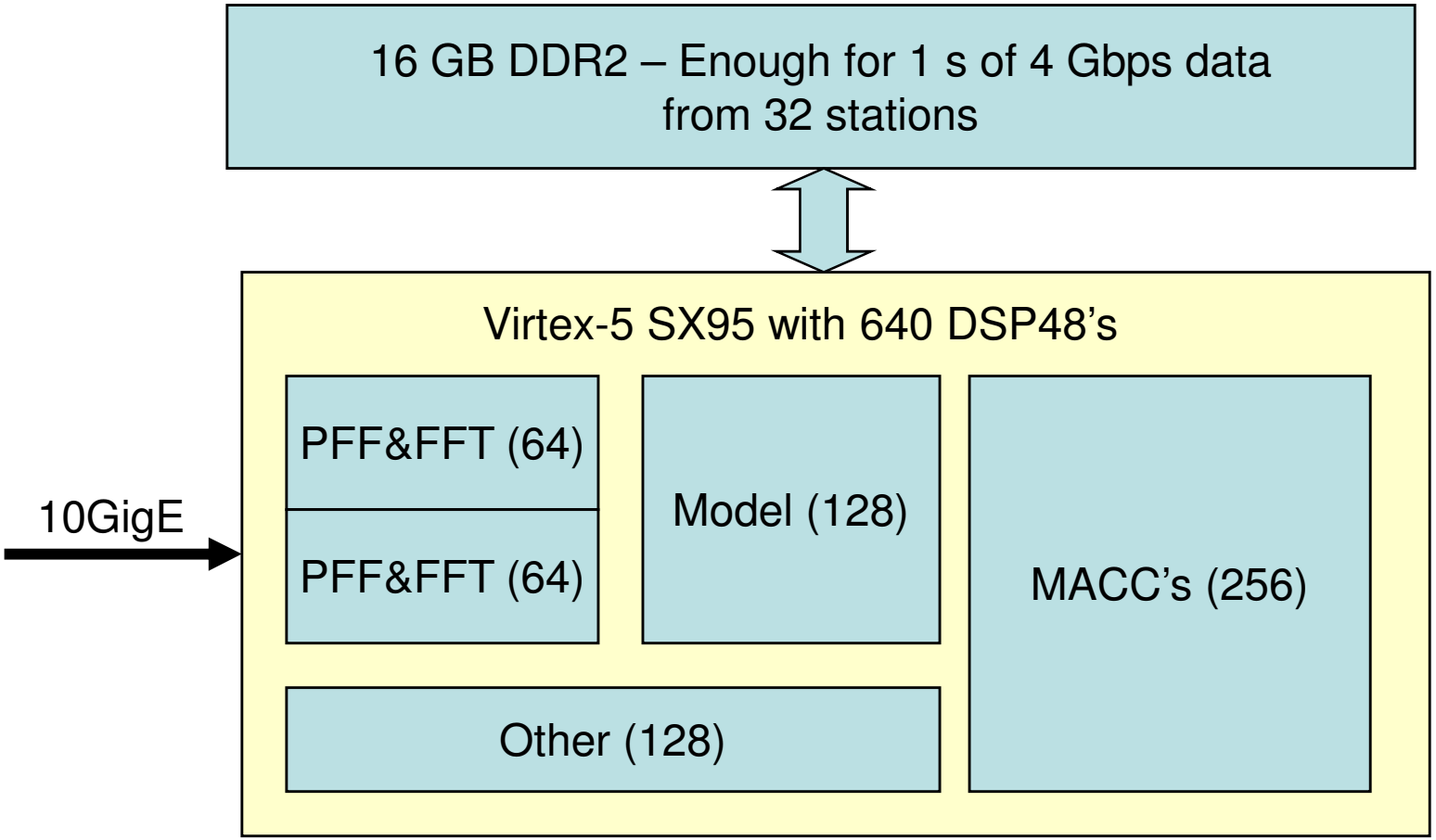
What is a hybrid correlator?

- Involves the use of a flexible custom FPGA accelerator board along with the usual computers and data routers of a software correlator.
- Consider an example of a hybrid correlator based on the DBE2.

DBE2 correlator accelerator board - complete correlator-on-a-board



How many DBE's are needed?

With respect to FFT's

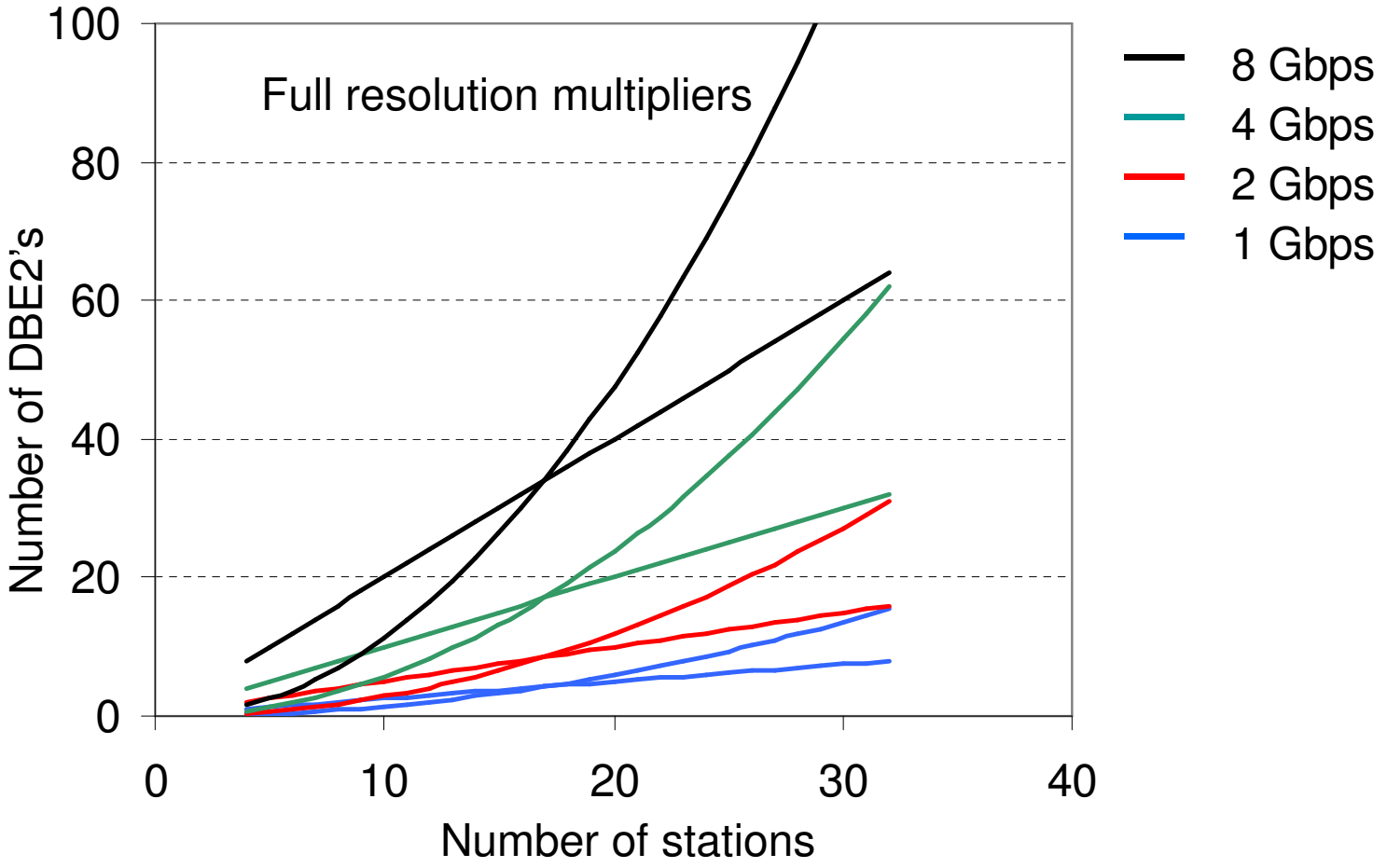
$$(N_{board} \cdot N_{FFT}) \cdot DRate_{FFT} = N_{Station} * \frac{DRate_{Sustained}}{n_{bit}}$$

With respect to MACC's

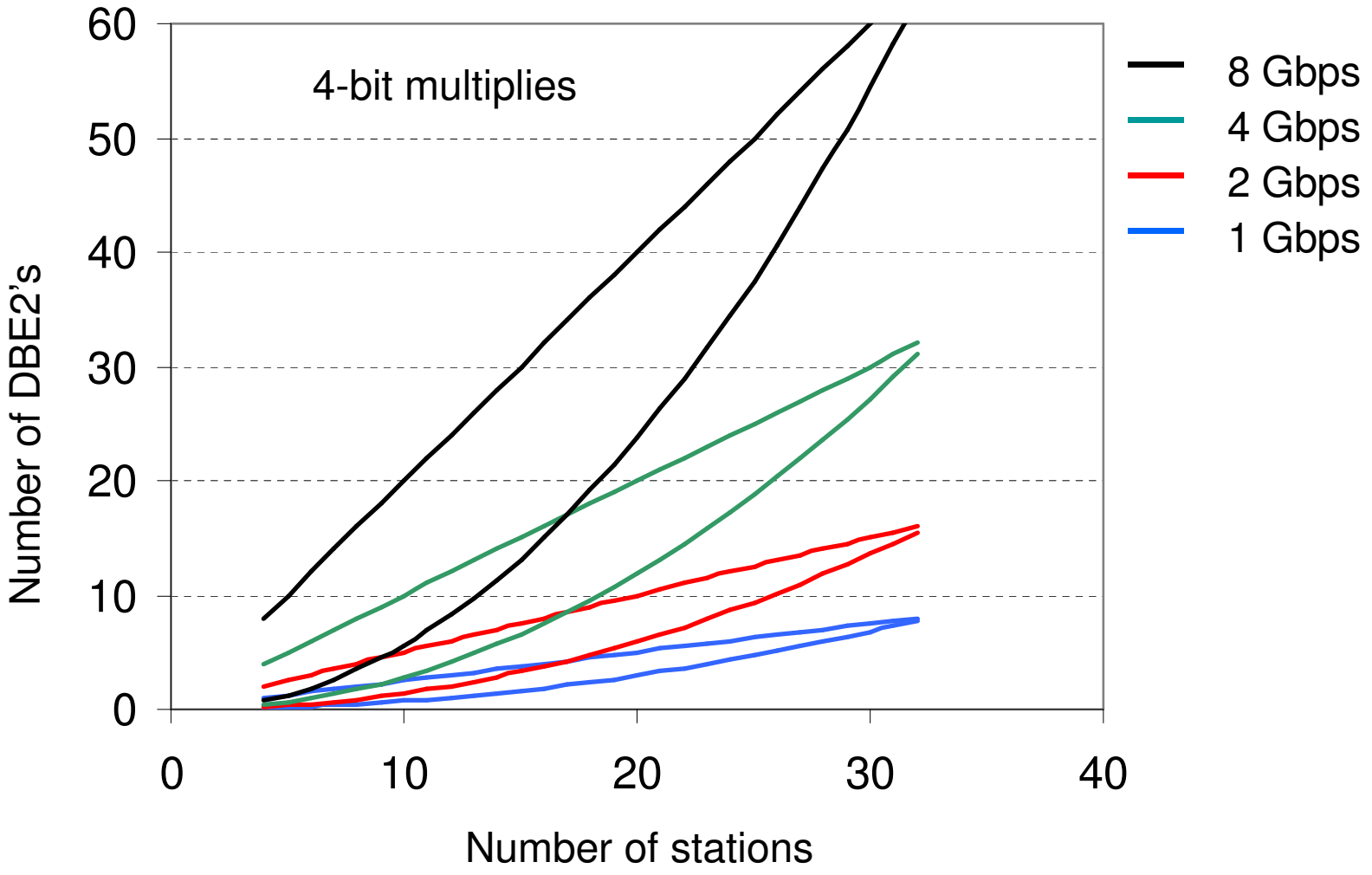
$$N_{Board} \cdot \frac{N_{MACC}}{N_{MACC}/bsl'n} \cdot DRate_{MACC} = \frac{N_{Stat} \cdot (N_{Stat} - 1)}{2} \cdot \frac{DRate_{Sustained}}{2 \cdot n_{bit} \cdot n_{pol}}$$

* The number of MACC's per baseline is 16 for full resolution multiplies and 8 for 4-bit multiplies

Number of DBE2's required assuming full resolution multipliers



Number of DBE2's required assuming 4-bit multipliers



Conclusion

- A complete 24-station correlator could be implemented with 35 DBE2's (25 if 4-bit multiplies are used)
- At ~$5K per DBE2 the correlator is economical and flexible.

[Note: These estimates are based on very rough estimates and could be a factor of several incorrect.]